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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SHAAWAT, MUSSA	
ART UNIT	**PAPER NUMBER**
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/707,486	PIPPIN, JACK D.
	Examiner	**Art Unit**
	Mussa A Shaawat	2128

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07 November 2000*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to application # 09/707,486, filed on November 07, 2000. Claims 1-40 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-9, 11-27, 31-37, and 39-40 are rejected under 35 U.S.C. 102(e) as being anticipated by John D. Kenny US Patent No. (5,287,292) referred to hereinafter as Kenny.

As to claim 1, Kenny teaches an integrated circuit comprising: a register to store a threshold temperature value (see col.5 lines 64-67, an up/down counter includes a register that stores the threshold value); a thermal sensor (see col.1 lines 54-56); and clock adjustment logic to decrease a clock frequency in response to the thermal sensor indicating that the threshold temperature value has been exceeded (see col.2 lines 3-28, et-seq.).

As to claim 2, Kenny teaches an integrated circuit of Claim 1 further comprising: threshold adjustment logic to increase the threshold temperature value to a new threshold temperature value in response to the thermal sensor indicating that the threshold temperature value has been exceeded (see col.2 lines 17-27).

As to claim 3, Kenny teaches an integrated circuit of Claim 2 wherein the threshold adjustment logic is further to increase the new threshold temperature in response to the thermal

sensor indicating that the new threshold temperature has been exceeded (see col.5 lines 64-67, and col.6 lines 1-14).

As to claim 4, Kenny teaches an integrated circuit of Claim 3 wherein the threshold adjustment logic is further to lower the new threshold temperature to detect decreases in temperature (see col.2 lines 3-16).

As to claim 5, Kenny teaches an integrated circuit of Claim 1 wherein the clock adjustment logic is to increase the clock frequency after a predetermined duration (see col.2 lines 37-47, the where sampling the clocking frequency of the IC at regular time intervals corresponds to a clock adjustment logic to increase the clock frequency after a predetermined duration).

As to claim 6, Kenny teaches an integrated circuit of Claim 1 wherein the clock adjustment logic is to increase the clock frequency in response to the thermal sensor indicating that the sensed temperature is less than the threshold temperature (see col.2 lines 18-47).

As to claim 7, Kenny teaches an integrated circuit of Claim 1 further comprising a fail-safe sensor and halt logic to halt operation of the integrated circuit in response to the fail-safe sensor indicating that a fail-safe threshold temperature has been exceeded (see col.1 lines 50-64, col.1-36, where the temperature detector and the temperature threshold inherently teaches a fail safe mode that will cause a halt operation).

As to claim 8, Kenny teaches an integrated circuit of Claim 7 wherein the halt logic is to inhibit operation of the integrated circuit by stopping a clock of the integrated circuit (see col.6 lines 15-23, col.1 lines 50-64, col.1-36, where the temperature detector and the temperature threshold inherently teaches a fail safe mode that will cause a halt operation).

As to claim 9, Kenny teaches an integrated circuit of Claim 7 wherein the fail-safe threshold temperature is a predetermined fixed critical temperature (see col.2 lines 17-27).

As to claim 11, Kenny teaches an integrated circuit of Claim 1 further comprising an interrupt handler to display information regarding the sensed temperature to a user of the integrated circuit (see col.2 lines 48-50).

As to claim 12, Kenny teaches an integrated circuit of Claim 1 further comprising interrupt logic to generate a first interrupt if the calculated average temperature exceeds a first threshold and a second interrupt if the calculated average temperature exceeds a second threshold (see col.2 lines 17-27).

As to claim 13, Kenny teaches an integrated circuit of Claim 1 wherein the clock adjustment logic executes instructions to vary the frequency of a clock signal of the integrated circuit in response to the thermal sensor (see col.2 lines 27-36).

As to claim 14, Kenny teaches an integrated circuit of Claim 1 wherein the clock adjustment logic executes instructions to provide closed loop control of the integrated circuit clock frequency, thereby automatically reducing the temperature when overheating occurs (see col.2 lines 36-47).

As to claim 15, Kenny teaches an integrated circuit of Claim 1 further comprising interrupt logic to activate an active cooling device in response to the thermal sensor (see col.1 lines 19-25, and col.1 lines 54-60, where a cooling fan corresponds to the cooling device).

As to claim 16, Kenny teaches a method comprising: storing a threshold temperature value in a register (see col.5 lines 64-67); sensing the temperature of an integrated circuit (see

col.1 lines 54-56); and decreasing a clock frequency of the integrated circuit in response to the sensed temperature exceeding the threshold temperature value (see col.2 lines 3-28, et-seq.).

As to claim 17, Kenny teaches a method of Claim 16 further comprising: increasing the threshold temperature value to a new threshold temperature value in response to the sensed temperature exceeding the threshold temperature value (see col.2 lines 17-27).

As to claim 18, Kenny teaches a method of Claim 17 further comprising increasing the new threshold temperature in response to the sensed temperature exceeding the threshold temperature value (see col.5 lines 64-67, and col.6 lines 1-14).

As to claim 19, Kenny teaches a method of Claim 16 further comprising lowering the new threshold temperature to detect decreases in temperature (see col.2 lines 3-16).

As to claim 20, Kenny teaches a method of Claim 16 further comprising increasing the clock frequency after a predetermined duration (see col.2 lines 37-47).

As to claim 21, Kenny teaches a method of Claim 16 further comprising increasing the clock frequency in response to the sensed temperature being less than the threshold temperature (see col.2 lines 18-47).

As to claim 22, Kenny teaches a method of Claim 16 further comprising displaying information regarding the sensed temperature to a user of the integrated circuit (see col.2 lines 48-50).

As to claim 23, Kenny teaches a method of Claim 16 further comprising executing instructions to vary the frequency of a clock signal of the integrated circuit in response to the sensed temperature (see col.2 lines 27-36).

As to claim 24, Kenny teaches a method of Claim 16 further comprising executing instructions to provide closed loop control of the integrated circuit clock frequency, thereby automatically reducing the temperature when overheating occurs (see col.2 lines 36-47).

As to claim 25, Kenny teaches a microprocessor comprising: a register storing a register value corresponding to a threshold temperature (see col.5 lines 64-67); a programmable thermal sensor receiving the register value, wherein the programmable thermal sensor generates a first interrupt signal if a microprocessor temperature exceeds the threshold temperature corresponding to the register value (see col.1 lines 54-56); clock circuitry to provide a clock signal for the microprocessor (see col.2 lines 56-67); and a processor unit coupled to the clock circuitry, wherein the processor unit executes instructions to vary the frequency of the clock signal in response to the first interrupt (see col.2 lines 18-47).

As to claim 26, Kenny teaches a microprocessor of claim 25 further comprising a fail-safe thermal sensor generating a fail-safe interrupt signal if the microprocessor temperature exceeds a fail-safe threshold temperature, wherein the processor unit is halted in response to the fail-safe interrupt signal (see col.1 lines 50-64, col.1-36, where the temperature detector and the temperature threshold inherently teaches a fail safe mode that will cause a halt operation).

As to claim 27, Kenny teaches a microprocessor of claim 25 wherein the clock circuitry further comprises a phase locked loop (see col.2 lines 36-47).

As to claim 31, Kenny teaches a microprocessor of claim 25 wherein the processor executes instructions to reduce a frequency of the clock signal in response to the first interrupt signal (see col.2 lines 27-36).

As to claim 32, Kenny teaches a microprocessor of claim 25 wherein the processor executes instructions to provide closed loop control of the microprocessor clock frequency, thereby automatically reducing the temperature when overheating occurs (see col.2 lines 36-47).

As to claim 33, Kenny teaches a microprocessor of claim 25 wherein the clock circuitry further comprises: a first clock; a frequency divider coupled to the first clock to provide the clock signal, the frequency divider reducing a frequency of the clock signal in response to the interrupt signal; and a second clock circuit coupled to provide the clock signal to the microprocessor (see col.2 lines 56-67).

As to claim 34, Kenny teaches a microprocessor of claim. 25 wherein the processor unit programs the register with another register value corresponding to another threshold temperature in response to the first interrupt signal (see col.5 lines 64-67, and col.6 lines 1-14).

As to claim 35, Kenny teaches a method of controlling a temperature of a microprocessor, comprising: generating a temperature signal within the microprocessor indicative of the temperature of the microprocessor (see col.2 lines 3-28, et-seq.); comparing the temperature signal with a first threshold temperature level within the microprocessor (see col.2 lines 3-28, et-seq.); generating an interrupt signal if the temperature signal indicates that the first threshold temperature level has been exceeded (see col.5 lines 64-67, and col.6 lines 1-14); and decreasing a microprocessor clock frequency in response to the interrupt signal (see col.2 lines 3-16).

As to claim 36, Kenny teaches a method of claim 35 further comprising: comparing the temperature signal with a second threshold temperature level, wherein the second threshold

temperature level represents a fail-safe temperature; and halting the microprocessor, if the temperature signal indicates that the second threshold temperature level has been exceeded (see col.1 lines 50-64, col.1-36).

As to claim 37, Kenny teaches a method of claim 35 further comprising: generating a fail-safe interrupt signal if the microprocessor temperature exceeds a fail safe threshold temperature; and halting the microprocessor in response to the fail-safe interrupt signal (see col.1 lines 50-64, col.1-36).

As to claim 39, Kenny teaches a method of claim 35 further comprising providing closed loop control of the microprocessor clock frequency, thereby automatically reducing the temperature when overheating occurs (see col.2 lines 36-47).

As to claim 40, Kenny teaches a method of claim 35 further comprising programming the microprocessor with a second threshold temperature in response to the first interrupt signal (see col.2 lines 1-36).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over John D. Kenny US Patent No. (5,287,292) referred to hereinafter as Kenny in view of Stanley W. Joehlin US Patent No. (4,807,144) referred to hereinafter as Joehlin.

As to claim 10, Kenny teaches a thermal sensor placed across an integrated sensor (see col. 1 lines 54-56), and an average mechanism to calculate the average temperature (see col.8 lines 57-67). Kenny does not expressly teach a plurality of thermal sensors and a mechanism to calculate the average temperature from the plurality of thermal sensors.

However Joehlin teaches one or more temperature sensors (see col.1 lines 41-43) and a system for calculating the average temperature for the set of temperature values (see col.7 lines 6-10, and Figure 5).

It would have been obvious to one of the ordinary skill in the art at the time of the applicant's invention to combine the teaching Joehlin to Kenny's method because Joehlin's teaching of a plurality of thermal sensors and a mechanism to calculate the average temperature for the set of temperature values would allow users of Kenny's method to improve the manufacturing operation of an integrated circuit by monitoring and controlling the heat generation of the integrated circuit so that it would not cause any damage to the integrated circuit.

4. Claims 28-30, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over John D. Kenny US Patent No. (5,287,292) referred to hereinafter as Kenny as applied to the rejection of claims 25 and 35 above in view of Hitoshi Kinoshita US Patent No. (5,149,199) referred to hereinafter as Kinoshita.

As to claim 28, Kenny teaches a thermal sensor (see col. 1 lines 54-56).

Kenny does not expressly teach a current source; a voltage reference coupled to the current source to provide a bandgap reference voltage, wherein the bandgap reference voltage is

substantially constant over a range of temperatures; an output voltage varying with the microprocessor temperature in accordance with the register value; and a comparator, wherein the comparator generates the first interrupt signal if ,a difference between the output voltage and the bandgap reference voltage indicates that the threshold temperature has been exceeded.

However Kinoshita teaches a current source; a voltage reference coupled to the current source to provide a bandgap reference voltage, wherein the bandgap reference voltage is substantially constant over a range of temperatures (see col.3 lines 1-4, where the first current source flowing into a bandgap type voltage);

An output voltage varying with the microprocessor temperature in accordance with the, register value (see col.3 lines 5-6, where the second source corresponds to the output voltage changing with temperature); and

A comparator (see col.3 line 7), wherein the comparator generates the first interrupt signal if a difference between the output voltage and the band9ap reference voltage indicates that the threshold temperature has been exceeded (see col.3 lines 26-30, where the amount of current from the first and second current sources change after they have reached a preset values corresponds to generating an interrupt signal if a difference between the output voltage = second source and the bandgap voltage=first source occurs).

It would have been obvious to one of the ordinary skill in the art at the time of the applicant's invention to combine the teaching Kinoshita to Kenny's method because Kinoshita's teaching of the use of a bandgap type voltage source and a comparator would allow users of Kenny's method to improve the manufacturing operation of an integrated circuit by monitoring

and controlling the heat generation of the integrated circuit so that it would not cause any damage to the integrated circuit.

As to claim 29, Kenny teaches a thermal sensor to monitor the temperature of the integrated circuit (see col. 1 lines 54-56).

Kenny does not expressly teach a transistor coupled to the current source, a gain ratio of the output voltage to a junction voltage of the transistor controlled by a transistor bias, wherein the junction voltage varies in accordance with a junction temperature of the transistor, a bias circuit providing the transistor bias to control the gain ratio, wherein the output voltage varies with the microprocessor temperature in accordance with the register value.

However Kinoshita teaches a transistor coupled to the current source (see col.4 lines 30-31), a gain ratio of the output voltage to a junction voltage of the transistor controlled by a transistor bias (see col.4 lines 49-55,), wherein the junction voltage varies in accordance with a junction temperature of the transistor (see col.6 lines 1-15), a bias circuit providing the transistor bias to control the gain ratio (see col.4 lines 50-55), wherein the output voltage varies with the microprocessor temperature in accordance with the register value (see col.3 lines 26-30, where generating heat can be changed by changing the amount of current flowing through the first=bandgap voltage and second=output voltage current sources corresponds to the output voltage being varied with the changing temperature).

It would have been obvious to one of the ordinary skill in the art at the time of the applicant's invention to combine the teaching Kinoshita to Kenny's method because Kinoshita's teaching of the use of a bandgap type voltage source and a comparator would allow users of Kenny's method to improve the manufacturing operation of an integrated circuit by monitoring

and controlling the heat generation of the integrated circuit so that it would not cause any damage to the integrated circuit.

As to claim 30, Kenny teaches a thermal sensor (see col. 1 lines 54-58). Kenny does not expressly teach a bias circuit that comprises weighted resistors.

However Kinoshita teaches a bias circuit that comprises weighted resistors (see col.4 lines 66-67).

It would have been obvious to one of the ordinary skill in the art at the time of the applicant's invention to combine the teaching Kinoshita to Kenny's method because Kinoshita's teaching of the use of a bandgap type voltage source and a comparator would allow users of Kenny's method to improve the manufacturing operation of an integrated circuit by monitoring and controlling the heat generation of the integrated circuit so that it would not cause any damage to the integrated circuit.

As to claim 38, the limitations of claim 38 are similar to the limitations of claim 28; therefore it is rejected based on the same rationale, supra.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicants disclosure.

- Ohmori US Patent No. (5,477,417) Electronic equipment having integrated circuit device and temperature sensor.
- Atriss US Patent No. (5,359,234) Circuit and method of sensing and temperature variation in an integrated circuit.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mussa A Shaawat whose telephone number is (571) 272-3785. The examiner can normally be reached on Monday-Friday (8:30am to 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R Homere can be reached on (571) 272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mussa Shaawat
Patent Examiner
December 14, 2004

JEAN R. HOMERE
PRIMARY EXAMINER